## REMARKS

Reconsideration of this application as amended is respectfully requested. Claims 38-50 are pending in the application, and all stand rejected. Claims 38 and 40 are amended and new claims 44-51 have been added.

Claim 38 stands rejected under 35 U.S.C. 102(b) as being anticipated by Manning, U.S. patent No. 5,729,503 ("Manning"). However, the Office Action has failed to show a prima facie case of anticipation, and Claim 38 as amended should therefore be allowed.

" [F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention ..." MPEP 706.02 (emphasis added). " The identical invention must be shown in as complete detail as contained in the ... claim." *Richardson v., Suzuki Motor Co.*, 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Manning simply fails to disclose every aspect of the claimed invention.

Manning discloses a memory device designed to perform high speed **burst** access read and write cycles. (Manning, Abstract). In the burst mode of operation, multiple data values can be sequentially written to or read from the device in response to a single address location and multiple access cycle strobes. (Manning, Col. 1, l. 60-63). Significantly, the burst length is predefined. "[The] burst sequence of data continues for each/CAS falling edge until a *predetermined number of data accesses equal to the burst length occurs*." (Manning, Col. 4, l. 54-57, emphasis added). *See also* Manning, col. 5, l. 6-12 ("*predetermined* number of burst access writes are performed" ... "[a]fter the *predetermined* number of burst writes occur ...") (emphasis added). A burst mode to write a predetermined amount of data, reflecting the predetermined burst length *not* a "program mode" as described by Applicants and claimed in Claim 38

In contrast, Applicants disclose a method of programming a memory. (Application, Summary of the Invention, p. 5). A "fast program mode" allows programming of memory. (Application, p. 8, l. 6-10). The amount of data to be written during programming is *not* fixed. "[T]he block architecture of certain flash devices

allows a user to erase and update *only certain blocks or the entire chip.*" (Application, p. 7, lines 15-16). Accordingly, the program mode disclosed and claimed by Applicants is not disclosed by Manning, which merely discloses a fixed-length burst mode. For at least this reason, the Office Action fails to make out a prima facie case of anticipation regarding Claim 38. The rejection of Claim 38 should therefore be withdrawn. Also for the foregoing reasons, at least, all claims that depend from Claim 38, including claims 39-43, should also be allowed.

Also regarding Claim 38, Manning fails to disclose, suggest or teach programming a first piece of data at a first address in response to a pulse of a write signal. Manning also fails to disclose, teach or suggest programming a second piece of data at a second address in response to a pulse of a write signal. In fact, Manning clearly teaches away from such limitations.

Manning discloses that pulsing of the write signal is eliminated (*See* Summary of Invention, col. 2, l. 61-63: "Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds"). Manning clearly requires that the write enable line ***not*** be pulsed during a burst write: "The level of the /WE signal *must remain high* for read and low for write burst accesses throughout the burst access." Manning, col. 5, l. 39-43 (emphasis added). "For burst writes, /WE transitions to high to terminate a current burst write access ..." Manning, col. 5, l. 67 – col. 6, l. 2.

In contrast, claim 38 claims programming a first piece of data at a first address in response to a pulse of a write signal and programming a second piece of data at a second address in response to a pulse of a write signal. Applicants disclose at p. 16 of the Application that "[a] write enable pulse to the flash component at step 650 causes the actual program algorithm to occur ... [e]ach time a write enable signal is sent to the flash component, logic in the flash device latches the data and programs that data ..." Application, p. 16, lines 16-22. Applicants disclose that a write enable signal, 704, is toggled to generate a pulse713, 714, 715, 721, 724 on the write enable signal; these pulses cause programming of the memory component to occur. Fig. 7; pp. 18-21. For at least

this reason, Claim 38 and all its dependent claims are allowable because the Office Action fails to make out a prima facie case of anticipation regarding Claim 38.

Manning's reliance on a pulse of the write enable signal to terminate a burst transmission also presents a second reason that a prima facie case of anticipation is not made out with respect to Claim 38. That is, Manning teaches that pulsing of the write enable signal terminates a burst mode transmission (see discussion above). Accordingly, Manning fails to teach "checking whether termination of said fast program mode is indicated" by "detecting if an incoming address is different from said first address" as claimed in Claim 38. Claim 38 is therefore allowable for at least this reason, as are all claims that depend from Claim 38.

Manning also fails to disclose, teach or suggest a method of programming flash memory, as claimed in new claim 44. Manning merely discloses writing data to a burst memory device, such as a DRAM. (See Manning, col. 1, l. 59-63: "It is desirable to design and manufacture a memory device having a standard DRAM pinout and a burst mode of operation ...") In contrast, Applicants disclose loading code and/or data into a flash memory component. Application, p. 10, l. 10; p. 10, l. 15; Fig. 4. One of skill in the art would not have been led to apply the teachings of Manning, which are specifically directed to burst-mode DRAM devices, to the problem of improving programming times and clock frequency associated with programming flash memory (*See* Application, p. 7, l. 21 – p. 8, l). Manning thus fails to disclose, teach or suggest all limitations of Claim 44. Claim 44 is thus allowable for at least the forgoing reasons. Similarly, all claims that depend from Claim 44 are also in condition for allowance.

Claim amendments, other than those specifically discussed above, were voluntarily made to broaden the scope of the Claims.

In summary, for the reasons noted above, Claims 38-51 are distinguished over the cited art and are in condition for allowance. It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. Favorable action is respectfully solicited. Allowance of the Claims is respectfully requested.

The Examiner is invited to call Shireen Bacon, Reg. No. 40,494, at 512-314-0435 if there remains any issue with allowance of this case.

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Respectfully submitted,

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